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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,367	09/14/2004	Timothy H. Daubenspeck	BUR920040154US1	5366

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SCHMEISER, OLSEN & WATTS
22 CENTURY HILL DRIVE
SUITE 302
LATHAM, NY 12110

EXAMINER	
AU, BAC H	
ART UNIT	**PAPER NUMBER**
2822	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/711,367	DAUBENSPECK ET AL.	
	Examiner	Art Unit	
	Bac H. Au	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28,30-32 and 34-36* is/are pending in the application.

4a) Of the above claim(s) *18-28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17,30-32 and 34-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on December 27, 2006, in which claims 1, 2, 8, 9 and 30, 31, and 34-36 were amended, and claims 29 and 33 were cancelled has been entered.

Claim Objections

2. Claims 24, 30 and 34 are objected to because of the following informalities:

Withdrawn claim 24 is mis-labeled as claim 25; consequently, there are two claims 25.

Regarding claim 30, "~~second~~ conformal" in line 2 should be --second ~~conformal~~--.

Regarding claim 34, "second conformal" in line 2 should be --second ~~conformal~~--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 30 and 34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In both claims 30 and 34, lines 2-3 "a top surface of said first dielectric layer surrounding a top surface of second dielectric layer... being coplanar" does not make

sense since the first dielectric layer is over the second dielectric layer. The claims are interpreted as --after the step of completely removing said dielectric layer from top surfaces of said wire bond pads, a top surface of said second dielectric layer surrounding a top surface of first dielectric layer... being coplanar with each other, and parallel to said top surface of said substrate--.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 4, 6-8, 13, 15-16, 30-31, and 34-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Banerjee (U.S. Pat. 6566757).

Regarding claims 1 and 8, Banerjee [Figs.5-7] discloses a method, comprising:

(a) providing a substrate [102];

(b) forming a passivation layer on a top surface of said substrate [Col.4 lines 42-48];

(c) forming an electrically conductive layer [104] on a top surface of said substrate; passivation layer;

(d) patterning said conductive layer into a plurality of wire bond pads spaced apart; top surfaces of said wire bond pads coplanar after said patterning; said top surface of said substrate exposed between said wire bond pads, top surfaces of said

wire bond pads being top surfaces of said conductive layer; a top surface of said conductive layer and top surfaces of said wire bond pads being a same surface, said top surfaces being parallel to said top surface of said substrate [Col.4 lines 42-48];

after said patterning; after said step (d); (e) forming a dielectric layer [103,107,108] directly on said top surface of said substrate; said passivation layer; in spaces between adjacent wire bond pads and directly on said top surfaces of said wire bond pads; said dielectric layer filling said spaces; and

after said forming said dielectric layer; after step (e); (f) completely removing said dielectric layer [103,107,108] from said top surfaces of said conductive layer of said wire bond pads, top surfaces of said dielectric layer in said spaces coplanar with said top surfaces of said wire bond pads [Fig.6].

Regarding claims 4, 6-7, 13, 15-16, 30-31, and 34-36, Banerjee [Figs.5-7] discloses a method,

forming a final dielectric layer [113] on said substrate, said dielectric layer and said wire bond pads; and

forming openings [110] in said final dielectric layer to expose less than an entire portion of each said wire bond pad [104] in said openings;

wherein said dielectric layer [103,107,108] comprises a layer of silicon oxide, a layer of silicon nitride or combinations thereof [Col.4 lines 60-67];

wherein said wire bond pads [104] comprise aluminum, aluminum copper alloy, copper, gold, tantalum, tantalum nitride or combinations thereof [Col.4 lines 42-48];

wherein said dielectric layer comprises a first dielectric layer [108] over a second dielectric layer [103], after the step of completely removing said dielectric layer from said top surfaces of said wire bond pads, a top surface of said second dielectric layer surrounding a top surface of first dielectric layer, said top surfaces of said first and second dielectric layers being coplanar with each other, and parallel to said top surface of said substrate [Fig.6];

wherein said top surfaces of both said first and second dielectric layers are coplanar with said top surfaces of said wire bond pads [Fig.6];

wherein step (e) includes: depositing said dielectric layer [103,107,108] on top of said plurality of wire bond pads, said dielectric layer filling said spaces between said adjacent wire bond pads [Fig.5]; and

planarizing said dielectric layer in order to coplanarize said top surface of dielectric layer and said top surfaces of said wire bond pads [Fig.6].

5. Claims 1, 8, 17, and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Yabu (U.S. Pat. 5989992).

Regarding claims 1 and 8, Yabu [Figs.16-17] discloses a method, comprising:

(a) providing a substrate [Col.6 line 66 – col.7 line 12];

(b) forming a passivation layer [Inherent] on a top surface of said substrate [Col.6 line 66 – col.7 line 12];

(c) forming an electrically conductive layer [12] on a top surface of said substrate; passivation layer;

(d) patterning said conductive layer into a plurality of wire bond pads spaced apart; top surfaces of said wire bond pads coplanar after said patterning; said top surface of said substrate exposed between said wire bond pads, top surfaces of said wire bond pads being top surfaces of said conductive layer; a top surface of said conductive layer and top surfaces of said wire bond pads being a same surface, said top surfaces being parallel to said top surface of said substrate [Fig.17(a)];

after said patterning; after said step (d); (e) forming a dielectric layer [13] directly on said top surface of said substrate; said passivation layer; in spaces between adjacent wire bond pads and directly on said top surfaces of said wire bond pads; said dielectric layer filling said spaces [Col.17 lines 45-48]; and

after said forming said dielectric layer; after step (e); (f) completely removing said dielectric layer [13] from said top surfaces of said conductive layer of said wire bond pads, top surfaces of said dielectric layer in said spaces coplanar with said top surfaces of said wire bond pads [Fig.17(b)].

Regarding claims 17 and 32, Yabu [Figs.16-17] discloses a method

further including between steps (b) and (c), forming via openings in said passivation layer exposing regions of electrically conductive wires in said substrate;

wherein step (d) fills said via openings with said electrically conductive layer; and

wherein step (d) includes forming each wire bond pad over at least one said via opening [Col.6 line 66 – col.7 line 12 discloses a semiconductor device including transistors and multiple layers of insulating films and metal wires. It would appear that these limitations are inherently disclosed.];

wherein said removing said dielectric layer includes: performing a chemical-mechanical polishing [Col.17 lines 48-50].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Banerjee (U.S. Pat. 6566757) in view of Shroff (U.S. Pat. 6500750).

Regarding claims 2, and 9, Banerjee discloses electrical interconnects and aspects of integrated circuit manufacturing as discussed above, but fail to explicitly disclose wherein the method further including: recessing said dielectric layer in said spaces below said top surfaces of said wire bond pads, an upper region of sidewalls of

said bond pads exposed in said spaces and a lower region of said sidewalls of said bond pads covered by said dielectric layer.

However, Shroff [Figs.1-3] discloses a method wherein further including: recessing said dielectric layer [1243] in said spaces below said top surfaces of said wire bond pads [1244], an upper region of sidewalls of said bond pads exposed [201] in said spaces and a lower region of said sidewalls of said bond pads covered by said dielectric layer [Col.4 lines 29-37].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Shroff into the method of Banerjee to provide recessing said dielectric layer in said spaces below said top surfaces of said wire bond pads, an upper region of sidewalls of said bond pads exposed in said spaces and a lower region of said sidewalls of said bond pads covered by said dielectric layer. The ordinary artisan would have been motivated to modify Banerjee in the manner set forth above for at least the purpose of improving alignment capabilities and reducing overlay errors in subsequent patterning operation [Shroff; col.4 lines 57-61].

7. Claims 5 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Banerjee (U.S. Pat. 6566757) in view of Bohr (U.S. Pub. 2002/0064929).

Regarding claims 5 and 14, Banerjee fails to disclose wherein said final dielectric layer comprises a material selected from the group consisting of polyimide and photo-sensitive polyimide. However, Bohr [Paras.33-34] discloses wherein said final dielectric

layer [218 of Fig.2g] comprises a material selected from the group consisting of polyimide and photo-sensitive polyimide.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Bohr into the method of Banerjee to include wherein said final dielectric layer comprises a material selected from the group consisting of polyimide and photo-sensitive polyimide.

The ordinary artisan would have been motivated to look to analogous art teaching alternative suitable or useful methods of performing the disclosed steps set forth above. Art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

8. Claims 3 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yabu (U.S. Pat. 5989992).

Regarding claims 3 and 10, Yabu [Figs.16-17] fails to disclose a method further including recessing said wire bond pads below said top surfaces of said dielectric layer in said spaces after said completely removing said dielectric layer from said top surfaces of said wire bond pads. However, Yabu [Figs.5 and 7; col.11 lines 25-32] discloses a method further including recessing said wire bond pads [15] below said top surfaces of said dielectric layer [20] in said spaces after said completely removing said dielectric layer from said top surfaces of said wire bond pads.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Figs.5 and 7 into the method of

Yabu Figs. 16-17 to include recessing said wire bond pads below said top surfaces of said dielectric layer in said spaces after said completely removing said dielectric layer from said top surfaces of said wire bond pads.

The ordinary artisan would have been motivated to look to analogous art teaching alternative suitable or useful methods of performing the disclosed steps set forth above. Art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

9. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yabu (U.S. Pat. 5989992) in view of Bohr (U.S. Pub. 2002/0064929).

Regarding claims 11-12, Yabu [Col.6 line 66 – col.7 line 12] discloses a semiconductor device including transistors and multiple layers of insulating films and metal wires, but fails to explicitly disclose a method further including

forming a final dielectric layer on said substrate; and

forming openings in said final dielectric layer to expose less than an entire portion of each said wire bond pad in said openings;

wherein said final dielectric layer comprises a material selected from the group consisting of polyimide and photo-sensitive polyimide.

However, Bohr [Fig.2g; paras.33-34] discloses a method further including

forming a final dielectric layer [218] on said substrate; and

forming openings [220] in said final dielectric layer to expose less than an entire portion of each said wire bond pad [222] in said openings;

wherein said final dielectric layer comprises a material selected from the group consisting of polyimide and photo-sensitive polyimide [Paras.33-34].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Bohr into the method of Yabu to include the claimed limitations. The ordinary artisan would have been motivated to modify Yabu in the manner set forth above for at least the purpose of proceeding to subsequent steps in the semiconductor device manufacturing process, as discussed by Yabu where the disclosed method is only an intermediate step and dealing with an intermediate wiring level.

Response to Arguments

10. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bac H. Au whose telephone number is 571-272-8795. The examiner can normally be reached on Mon-Fri 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BHA

Zandra V. Smith
Supervisory Patent Examiner
28 Feb. 2007